AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 9, line 14, as follows:

Figure 3 illustrates a hardware based instruction translator that may provide one embodiment of the invention. The hardware based instruction translator 22 includes hardware logic that recognises a particular slow form bytecode received. The instruction translator 22 may be present within the instruction processing pipeline of a processing system and accordingly will have access to the program counter address that is the bytecode address for the Java bytecode currently being translated. The bytecode address is represented as "BCAdd". Specific hardware 24 within the instruction translator 22 issues a lookup to the data cache 8 at the bytecode address BCAdd. If a Hit signal is returned, then this is accompanied by the replacement fast form instruction including its numeric reference and then this fast form instruction is used in place of the slow form instruction. In many cases, the fast form instruction is then passed from the instruction translator 22 to a complementary software interpreter as both the slow form instruction and the fast form instruction are too complex to be directly translated by the hardware translator 22. However, some fast form instructions are simple enough to be executed directly by the hardware translator 22, e.g. getfield_quick can be executed by hardware whereas the slow form is executed by software. Even though both of the slow form instruction and the fast form instruction are to be passed out to the software interpreter, the software interpreter is able to deal with the fast form instruction much more quickly

than the slow form instruction since it already includes a ~~resolve~~ resolved numeric address reference.